CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method comprising:
determining a power mode for a device;
disabling a phase locked loop by reducing power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode; and
providing the oscillator signal to an input of the phase locked loop and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode.

2. (Original) The method as in Claim 1, wherein the device consumes less power in the first power mode than in the second power mode.

3. (Previously Presented) The method as in Claim 1, further including suspending processing within the device when in a third power mode.

4. (Currently Amended) The method as in Claim 1, wherein the oscillator signal is generated through a crystal oscillator.

5. (Original) The method as in Claim 1, wherein the oscillator signal is generated through an RC circuit.

6. (Original) The method as in Claim 1, wherein the output of the phase locked loop is coupled to a clock divider and an output associated with the clock divider is coupled to the clock line.

7. (Previously Presented) The method as in Claim 6, wherein:

disabling the phase locked loop, when in the first power mode, includes providing the oscillator signal to the input of the clock divider; and

providing the oscillator signal to the phase locked loop, when in the second power mode, includes providing the locked signal to the input of the clock divider.

8. (Previously Presented) The method as in Claim 1, wherein disabling the phase locked loop, when in the first power mode, further includes providing reduced power, in comparison to an available power, to the device.

9. (Previously Presented) The method as in Claim 1, wherein disabling the phase locked loop, when in the first power mode, further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data.

10. (Canceled)

11. (Canceled)

12. (Previously Presented) The method as in Claim 9, wherein providing the oscillator signal to the phase locked loop, when in the second power mode, further includes using the maximum number of bits used to represent multimedia data.

13. (Original) The method as in Claim 1, wherein the device includes a portable device.

14. (Original) The method as in Claim 13, wherein the portable device includes a personal digital assistant.

15. (Previously Presented) The method as in Claim 1, wherein providing the oscillator signal to the phase locked loop, when in the first power mode, further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data.

16. (Original) The method as in Claim 15, wherein multimedia data includes video data.

17. (Original) The method as in Claim 15, wherein multimedia data includes audio data.

18. (Previously Presented) The method as in Claim 15, wherein disabling the phase locked loop, when in the first power mode, further includes using the maximum number of bits used to represent the multimedia data.

19. (Original) The method as in Claim 1, wherein disabling the phase locked loop includes shutting off power used for driving the phase locked loop.

20. (Currently Amended) The method as in Claim 1, wherein providing the oscillator signal to drive a clock line includes coupling a line carrying the oscillator signal to the clock line and wherein providing the locked signal from an output of the phase locked loop to the clock line includes decoupling the line carrying the oscillator signal from the clock line.

21. (Previously Presented) The method as in Claim 1, wherein determining the power mode includes identifying a number of pending instructions.

22. (Previously Presented) The method as in Claim 1, wherein determining the power mode includes identifying types of pending applications.

23. (Previously Presented) The method as in Claim 1, wherein determining the power mode includes identifying a change in display content.

24. – 35. (Canceled)

36. (Currently Amended) A computer readable medium tangibly embodying a program of instructions to manipulate a system to:

determine a power mode for the system;

disable a phase locked loop by shutting of power used for driving the phase locked loop and ~~providing~~ provide an oscillator signal to drive a clock line when in a first power mode; and

provide the oscillator signal to an input of the phase locked loop and ~~providing~~ provide a locked signal from an output of the phase locked loop to the clock line when in a second power mode.

37. (Original) The computer readable medium as in Claim 36, wherein the system consumes less power in the first power mode than in the second power mode.

38. (Previously Presented) The computer readable medium as in Claim 36, wherein the program of instructions is further used to:

represent multimedia data using a first number of bits when in the first power mode; and

represent multimedia data using a second number of bits when in the second power mode, wherein the first number of bits are less than the second number of bits.

39. (Original) The computer readable medium as in Claim 38, wherein the multimedia data includes video data.

40. (Original) The computer readable medium as in Claim 38, wherein the multimedia data includes audio data.

41. (Original) The computer readable medium as in Claim 36, wherein the power mode determined is based on a number of pending instructions.

42. (Original) The computer readable medium as in Claim 36, wherein the power mode determined is based on a change in display content.

43. (Original) The computer readable medium as in Claim 36, wherein the power mode determined is based on a type of instructions stored in the instruction buffer.

44. (Previously Presented) A system comprising:

a phase locked loop having a first input to receive a first clock signal and a first output to provide a second clock signal, wherein the second clock signal is based on the first clock signal;

a first multiplexer having a first input coupled to the first input of the phase locked loop, a second input coupled to the first output of the phase locked loop and an output, wherein the first multiplexer is operable to selectively provide to the output a signal received at the first input when in a first power mode or a signal received at the second input when in a second power mode; and

means for disabling the phase locked loop by reducing power used for driving the phase locked loop when in the first power mode.

45. (Previously Presented) The system as in Claim 44, further comprising:

a first clock divider having an input coupled to the output of the first multiplexer and an output coupled to a first bus.

46. (Previously Presented) The system as in Claim 45, further comprising:

a second multiplexer having a first input coupled to the first input of the phase locked loop, a second input coupled to the first output of the phase locked loop and an output, wherein the second multiplexer is operable to selectively provide to the output a signal received at the first input when in the first power mode or a signal received at the second input when in the second power mode; and

a second clock divider having an input coupled to the output of the second multiplexer and an output coupled to a second bus.

47. (Previously Presented) The system as in Claim 44, further comprising:
means for determining a power mode of the system; and
means for providing a control signal to the first multiplexer based on the determined power mode.

48. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a number of pending instructions.

49. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a type of pending instruction.

50. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a rate of change in a number of pending instructions.

51. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a change in display content.

52. (Previously Presented) The system as in Claim 44, wherein the means for disabling the phase locked loop includes means for shutting off a supply of power to the phase locked loop.

53. (Previously Presented) The system as in Claim 44, further comprising:
an oscillator having an output coupled to the first input of the phase locked loop, wherein the oscillator is operable to output the first clock signal.

54. (Previously Presented) The system as in Claim 53, further comprising means for disabling an output of the first clock signal by the oscillator when in the first power mode.

55. (New) The method as in Claim 1, wherein:

providing the oscillator signal to drive the clock line includes providing the oscillator signal to the clock line via a first input of a multiplexer; and

providing the locked signal from the output of the phase locked loop to the clock line includes providing the locked signal to the clock line via a second input of the multiplexer.

56. (New) The computer readable medium as in Claim 36, wherein:

providing the oscillator signal to drive the clock line includes providing the oscillator signal to the clock line via a first input of a multiplexer; and

providing the locked signal from the output of the phase locked loop to the clock line includes providing the locked signal to the clock line via a second input of the multiplexer.